ABSTRACT

A memory device and a method for refreshing the memory device. The memory device includes a memory cell capable of storing two bits of data. One bit is referred to as the normal data bit and the other bit is referred to as the complementary data bit. Each memory cell has an associated dynamic reference cell. The normal data is refreshed by latching refresh data into a data latch and ORing the latched data with input data. The refresh data is written to the corresponding memory location. The data for the complementary data bit is refreshed by latching complementary data bit refresh data into the complementary data latches and writing to the memory cell. The normal and complementary data bits are refreshed before each read operation.